**DIGITAL LOGIC DESIGN**

**LAB -13**

**Objective:** Student should understand how to design a sequential circuit given its specifications in sentence structure or state diagram or state table form. Furthermore undertand the use of shift registers and counters.

**Task #1:** Implement a synchronous up- down counter on logic trainer.

**Task #2:** Draw the logic diagram of a shift register with D flip flops with mode selection inputs S1 and S0 and implement the circuit on the breadboard. The shift register is to be operated according to the following function table. One stage of this register should contain a 4-to-1 line MUX and a D-type flip-flop.

|  |  |  |
| --- | --- | --- |
| **Mode Selection** | | **Register Operations** |
| **S1** | **S0** |
| 0 | 0 | No change |
| 0 | 1 | Shift right |
| 1 | 0 | Shift left |
| 1 | 1 | Parallel load data |

**POST LAB TASK:**

Analyze the given sequential circuit. Fill the table given below and mention the following:

1. Input equations
2. Output equations
3. Excitation equations
4. Next state equations
5. State diagram
6. Q
7. R

D Q

R

A

B

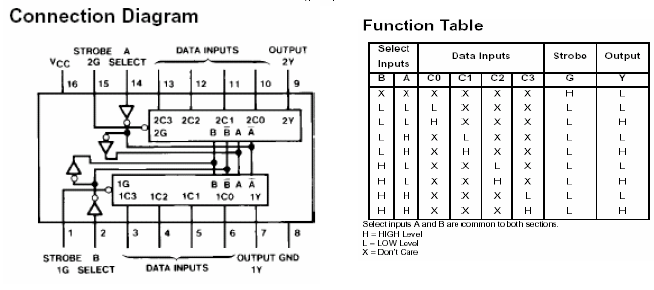
Q0

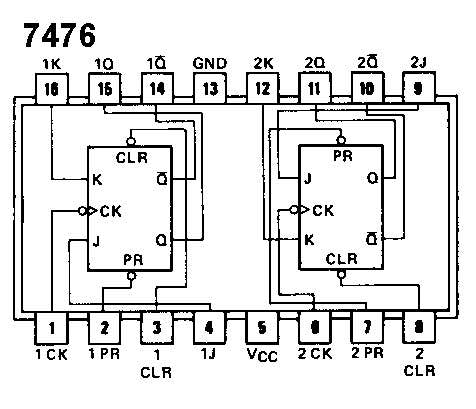
Q1

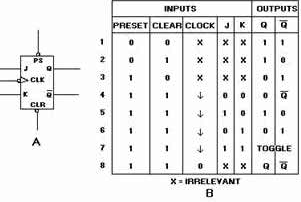
Z

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Current States** | | **Inputs** | | **Next States** | | **Output** |
| **Q0** | **Q1** | **A** | **B** | **Q0 (t+1)** | **Q1**  **(t+1)** | **Z** |
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**4 to 1 Mux:**



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